Demonstration of Photonically Controlled GaAs Digital/MMIC for RF Optical Links

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***Abstract*— We report design, fabrication, and test of a monolithic GaAs optoelectronic integrated circuit (OEIC) implementing a broad-band optically driven digital/analog radio frequency (RF) interface. The integrated circuit (IC) was fabricated using a foundry-compatible enhancement/depletion metal–semiconductor field-effect transistor (MESFET) process with no added lithography steps. A single optical fiber carries externally amplitude modulated 0.85-μm light to the on-chip GaAs metal–semiconductor–metal interdigitated photodetector. RF as well as simultaneous digital information encoded at up to 10 Mb/s using a novel waveform set is transmitted over the fiber. The serial digital data is self-clocked into on-chip registers to control the RF signal chain, which includes a three-bit digital attenuator. The circuit operates in an asynchronous mode to detect digital and RF on the single optical-fiber input, control RF level, and transmit the 2–8-GHz RF to the IC's electrical output. Measurements characterizing the RF and digital performance of the IC as well as a demonstration of the full optoelectronic mixed-mode functioning of the IC are presented.**

I. Introduction

LIGHTWAVE communications for local interconnections within a radio frequency (RF) system will yield savings in weight and simplified physical structure by replacing copper cabling and waveguide with optical fiber, provided the optical communications subsystem is optimized for the special needs of the RF system. Present-day RF systems require broad-band low-noise analog interconnections with tight control of effective line length (time delay/phase shift) as well as megabit/second digital links. The ubiquity of GaAs in RF systems and its good properties as a photodetector suggest use of a 0.85-μm wavelength that can be directly detected on a GaAs integrated circuit (IC). The economics of local interconnects in RF systems—hundreds or thousands of parallel short-haul links—are quite different from those of long-haul multiple-subscriber telecommunications. The low-cost on-chip integration possibility offered by the choice of a GaAs-compatible wavelength is the key.

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Relatively sophisticated GaAs-based optoelectronic integrated circuit (OEIC) technology has been available at the large scale integration (LSI) level for a number of years. As far back as 1989, a GaAs MESFET process was used to develop and demonstrate a digital optical receiver chip incorporating a metal–semiconductor–metal (MSM) photodetector and some 2500 additional devices, with a clock speed of 1 Gb/s [1]. In GaAs, higher bandwidth LSI technology has also been demonstrated. In an effort similar to that reported here, a GaAs MESFET-based OEIC incorporating an MSM photodetector and separate RF (6–8 GHz) and digital channels (125 Mb/s) was reported. Following the optical receiver and transimpedance amplifier, the digital channel included circuitry for clock recovery, data decoding/retiming, frame/symbol synchronization, and serial-to-parallel data conversion, while the RF channel was comprised of a four-stage lumped-element gain block. The digital and RF channels were subsequently separately taken off-chip [2]. By way of comparison, InP-based OEIC technology for 1.3–1.5-μm wavelength applications is only beginning to approach SSI levels of complexity. A long-wavelength (1.3 μm) monolithic receiver incorporating a p-i-n diode and seven JFET's in a cascode preamplifier operating at 622 Mb/s was reported in 1991 [3]. More recently, demonstrations of long-wavelength monolithic photoreceiver technology have extended the bandwidth to 10 Gb/s using six InAlAs/InGaAs high electron mobility transistors (HEMT's) with an on-chip p-i-n photodiode [4], and to 12 Gb/s incorporating six on-chip heterojunction bipolar transistors in the InGaAs–InP materials system [5]. A 10-Gb/s monolithic receiver incorporating a ridge waveguide, ridge waveguide PIN photodiode, and a transimpedance amplifier consisting of six InAlAs–InGaAs HEMT's has also been reported [6].

Even with the absence of the additional photonic devices, InP-based IC technology remains near the small-scale level of integration. The additional costs and complexity associated with the InP-based technology lead to the use of this materials system only when required by necessity of optical wavelength or low-noise high-frequency performance, and provide motivation for rapidly moving off-chip to more affordable GaAs or Si-based IC technology where possible.

At present, the 0.85-μm wavelength is clearly the only possibility for fully monolithic integration such as we report. Use of the more usual 1.3- or 1.5-μm wavelength would require an InGaAs/InAlAs/InP technology for the needed narrow-bandgap detectors, but monollithic microwave integrated cir-

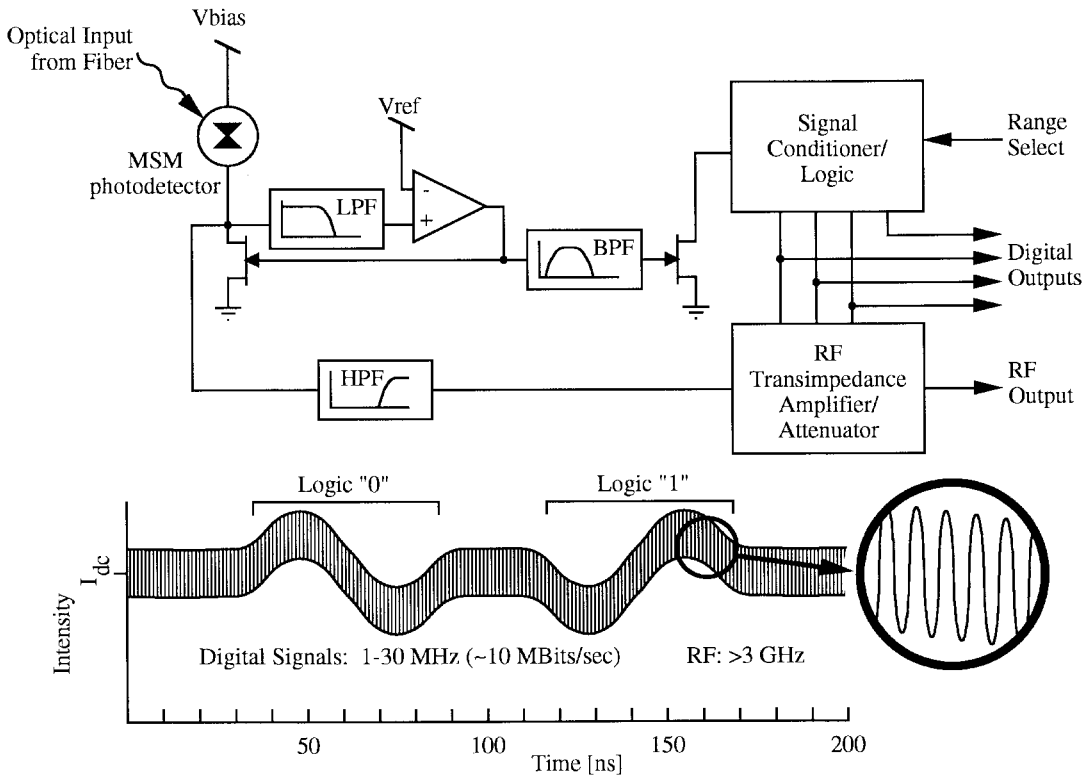


Fig. 1. Block diagram and schematic signals used for the MOE1 demonstration IC.

cuit (MMIC) technology will be dominated by processes based on the GaAs/AlGaAs semiconductor family until InP-based heterostructure foundry processes have reached a comparable level of maturity. The jury is out on whether this will ever happen; if experience on the replacement of Si by GaAs in LSI is any guide, it may not. GaAs has a stable niche in MMIC technology because its semi-insulating nature conveys a distinct qualitative advantage over Si rather than a merely incremental quantitative one. Since the advantage of InP over GaAs in the MMIC arena is mainly quantitative, the same market and technology forces which drove Si to increase its performance and exclude GaAs from the commodity very large scale integration (VLSI) arena may act to keep GaAs dominant in MMIC's. The large installed base of 1.3- and 1.5-μm technology does exert a strong pull on any optoelectronic link technology. However, monolithic integration confers significant cost and performance advantages on microwave links (thousands of which might be in a single radar system) whereas link lengths in such systems are so small that the low-loss advantage of longwave systems is mooted. Waiting until InP-based MMIC technology catches up to GaAs means deferring the cost advantages of monolithic integrability indefinitely. For this reason we have chosen to aggressively pursue a technology based on a wavelength, 0.85 μm, allowing monolithic integration.

To explore some of the capabilities of this technology we have designed, fabricated, and tested a photonic digital/RF monolithic interface IC suitable for use in a phased array, missile seeker, or other RF system needing broadband stable communication links implemented in an integrated, low-cost, lightweight, compact, foundry-compatible technology. The GaAs monolithic IC includes an on-chip MSM photodetector, low-frequency signal-conditioning circuitry, RF transimpedance amplification, a low-noise amplifier (LNA), a 3-b digitally controlled attenuator, and an error-detecting digital interface driving a serial-to-parallel converter which then controls the attenuator. We have demonstrated transmission of digital commands and continuous wave (CW) RF (as AM on an optical carrier at 0.85-μm wavelength) over a single fiber proximity coupled to the on-chip photodetector, and verified control of the output RF level in accordance with the simultaneously transmitted digital-serial commands. Inputs to the chip, in addition to the lightwave, were power and ground. Combining in a monolithic format optical detection, digital circuitry, and analog microwave circuitry controlled by the on-chip digital circuitry, this is the first IC of this type ever reported.

II. Design of the IC

The first stage in the design was selecting waveforms which would allow transmission of RF and digital data in separate frequency bands, and be simple to generate and decode. Fig. 1 shows a block diagram of the resulting microwave optoelectronic IC, MOE1, along with the chosen waveforms. The photocurrent generated in the MSM is comprised of an RF component ($>$2 GHz), a low-frequency digital component (LF, 1–30 MHz), and dc. In the amplifier shown following the low-pass filter, the dc and LF signals are amplified to produce a feedback voltage which is fed back to the gate of the main current-sink FET. Thus, the voltage at the drain of the main current-sink FET is stabilized against variations up to about 50

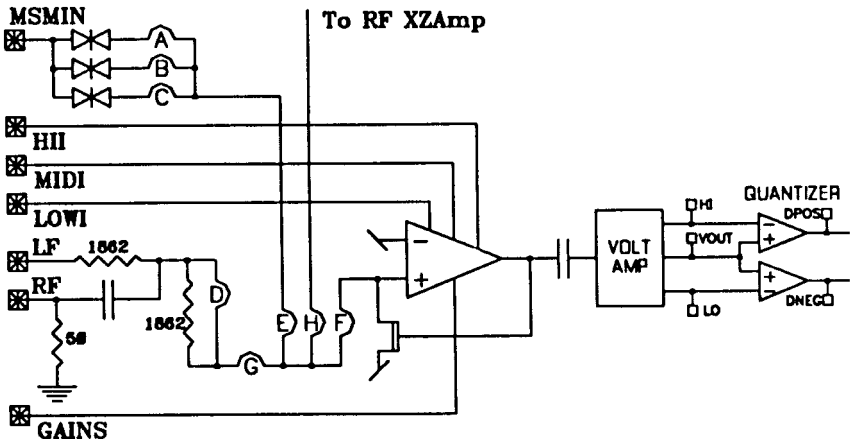


Fig. 2. Schematic detail of the front end of the MOE1 IC.

MHz, and the dc and LF photocurrent components are shunted through the FET. The feedback voltage is also bandpass-filtered to isolate the LF and amplified (with selectable gain set via a dc control input if desired) to provide the input to the logic signal conditioning circuitry. RF is outside the band of the feedback circuit and, therefore, appears across the drain impedance of the main FET. It is amplified by the RF chain and then fed to a 3-b digital attenuator. This attenuator is controlled by the output of the digital section.

Each serial digital data bit is encoded as a bipolar pulse pair comprising a band-limited single cycle of a 20-MHz sinewave. Depending on the starting phase (0° or 180°), a binary zero or one is encoded. The analog bandwidth required for the designed 10 Mb/s data rate is 1–30 MHz. Since we anticipated generating the optical modulation with a Mach–Zehnder modulator (MZM) biased in the linear region, a significant dc photocurrent (which carries no information) is allowed in addition to the two ac signal bands. Selection of a signaling waveform with no dc component simplifies design of the receiver and error detector as well, largely eliminating pattern-dependent bias shifts.

The detailed design of the IC allowed for many different modes of operation without different IC layouts. This was accomplished by including many airbridges which could be broken manually to select the particular configuration. For example, the entire analog front end can be isolated and the decode logic fed directly with pulse pairs. Likewise, the RF section's control inputs can be isolated from the on-chip circuitry and driven from pads. Since the interdigitated MSM photodetectors used offer performance tradeoffs depending on their linewidth and pitch, three different designs were included—each selectable via airbridge.

To simplify synthesizing test signals for electrically stimulating the circuit, an on-chip network was designed allowing separate test inputs for LF and RF signals, with good matching for the RF and isolation between the two inputs. Fig. 2 shows the front end of the IC in more detail, including the airbridges (named by various letters of the alphabet), allowing selection of test conditions. The four control inputs (HII, MIDI, LOWI, and GAINS) are digital inputs for selecting bias point and gain for the front end. These were included to allow for the possibility that the dynamic range at nominal gain would be less than anticipated. The small pads in the right-hand part of the figure are test-point outputs.

The digital signaling described above and shown in Fig. 1 uses a dc-free scheme with a high-low sequence for a logic one and a low-high for a logic zero. The coding scheme we use is not one of the standard ones but is fairly similar to Harvard (FM) encoding. (In fact, the present scheme is to Harvard encoding as NRZI is to NRZ. While it is phase-sensitive, it is not true Manchester-PM code.) The chosen waveform allows self-clocking, detection of noise pulses (high with no low, or vice versa), and clean separation of the frequency bands. Received digital pulse pairs with the proper timing are converted on-chip to digital bits accompanied by clock pulses. Each bit is shifted by means of its clock pulse into an on-chip shift register. The first bit must be a one. When it reaches the fourth register bit (i.e., after three more bits have been detected), on-chip circuitry generates a "LOAD" pulse which transfers bits 2, 3, and 4 from the shift register into the control register connected to the RF attenuator. One more received bit then shifts the leading one bit into the fifth register position, which engenders a "CLEAR" signal which zeroes the shift register (without affecting the control register) in preparation for the next command word. The entire process is asynchronous and self-clocked. No matter what state the chip wakes up in, a sequence of four "zero" bits will place the input register into a known (clear) state.

The RF chain starts with a transimpedance amplifier (XZAMP) to interface the low-power high-impedance RF voltage available at the drain of the main current-sink FET to the following RF circuitry, which is designed as 50-Ω blocks. The XZAMP is designed for a nominal gain of 40 dB$\cdot\Omega$, i.e., a transimpedance of 100 Ω. Its schematic is shown in Fig. 3. The XZAMP is followed by an LNA whose gain approximately cancels the insertion loss of the final RF circuit block, a digitally controlled three-bit attenuator.

The IC was designed to be fabricated on Raytheon Research Division's Enhancement/Depletion MESFET prototype line. This process is the basis for a foundry process now used in production at Raytheon. The process uses 0.5-μm gate length and yields enhancement/depletion (E/D) MESFET's

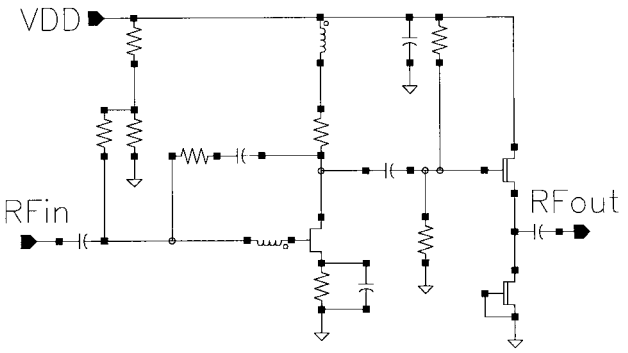


Fig. 3. Schematic diagram of the RF transimpedance amplifier.

with maximum f_T of 30 GHz and $f_{\max}$ above 60 GHz. The EFET and DFET channels are formed by selective ion implantation of Si and Be. The nominal threshold voltages for the EFET's and DFET's are $+0.1$ and -0.5 V, respectively. The source and drain ohmic contacts are formed on N^+ regions of the FET with a sheet resistance of 200 Ω/square. Gate material is Ti/Pt/Au and the recess depth is $\approx$400 Å. The process also features GaAs implanted resistors (which use unrecessed EFET channel implant) with a sheet resistance of 750 Ω/square, low-temperature coefficient ($<$200 ppm/K) 6-Ω/square TaN resistors, 300-pF/mm^2 MIM capacitors with 2000-Å SiN dielectric, air bridges, and low-loss inductors and transmission lines. The standard deviation of the threshold voltage is 22 mV across a given 3-in wafer. The maximum EFET transconductance is 275 mS/mm; the breakdown voltage is $\geq$9 V. Except for the gate, which is E-beam written, all lithography steps are done with an I-line stepper. The process includes two levels of interconnect Ti/Pt/Au metal with sheet resistances of 100 and 30 mΩ/square, respectively, the top level being used for 3-μm-thick transmission lines as well as digital interconnect. The process has been used to make IC's with both digital and MMIC circuitry on a single chip and has been used on a number of demonstration projects.

The planar structure of the MSM photodetector used on-chip is nearly ideal for RF/digital signal detection. Under time-varying illumination it acts as an almost ideal current source with high detection efficiency (0.41 A/W) and low capacitance ($\sim$50 fF). No extra masking layers were needed for the MSM detector interdigitated fingers, which were written on undoped GaAs (at the same time as the gates) with 0.5-μm linewidth on 1.0-, 1.5-, and 2.0-μm pitch.

III. Results

A photomicrograph of the completed IC is shown in Fig. 4. Running along the bottom of the photo is the digital circuitry. In the upper right of the photo are the three RF blocks with the attenuator on the right, adjacent to the distributed LNA, which is to the right of the XZAMP. There are some small test structures in the upper left corner (five 2 $\times$ 2 pad arrays) and just below them can be seen the three MSM's. The cross structure below and to the right of the MSM's is formed by the four airbridges G, E, F, and H (cf. Fig. 2).

The first tests carried out were RF characterization of the three RF blocks individually and of the whole, completed IC.

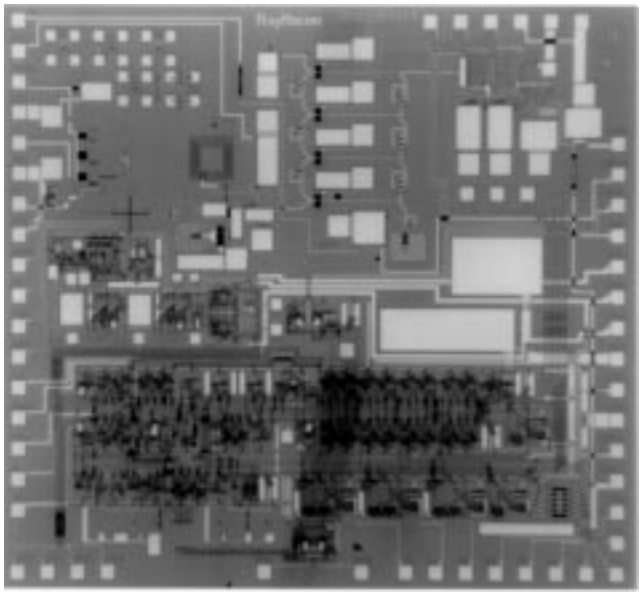


Fig. 4. The fabricated MOE1 IC.

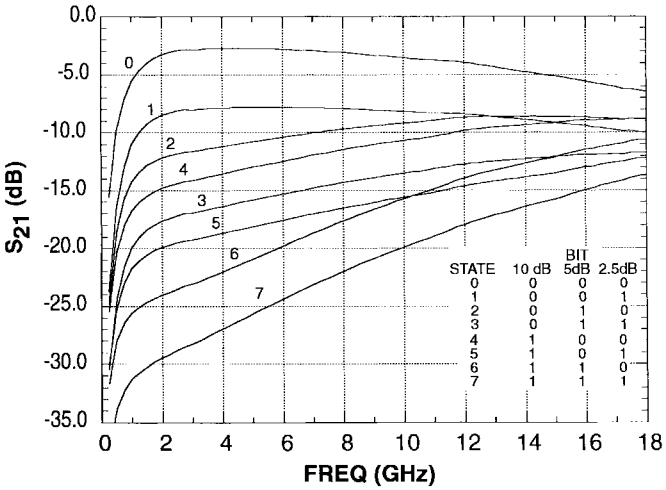


Fig. 5. Performance of a digitally controlled attenuator versus frequency.

Fig. 5 shows the results for the digitally controlled attenuator. At 3 GHz, where optically driven testing was done, the three bits show attenuation of 4.5, 7.5, and 10.0 dB, instead of the nominal design values of 2.5, 5.0, and 10.0 dB. The insertion loss in the lowest loss state is 3.0 dB. This first-cut design based on estimated models is not optimal, but is adequate for the proof-of-principle demonstration we present.

Fig. 6 shows a comparison between the whole-chip measurements and a model composed of the cascade of the three measured individual blocks. The good agreement shows that there are no surprises between RF blocks. However, to relate the RF measurements to the overall transimpedance is not simple.

The MSM produces a current largely independent of output voltage, and the RF output of the IC is power into a load, characterized as a voltage. The ratio of these two is the transimpedance, a parameter of great importance for the optoelectronic system designer since it affects the need for

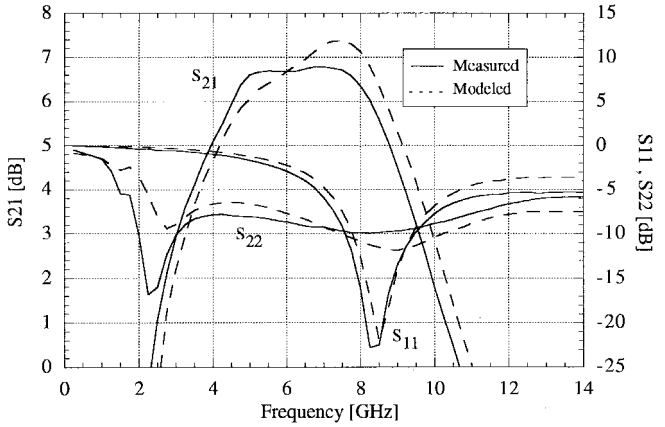


Fig. 6. Comparison of whole-chip RF S parameters with a model consisting of cascaded measurements of the three individual RF blocks.

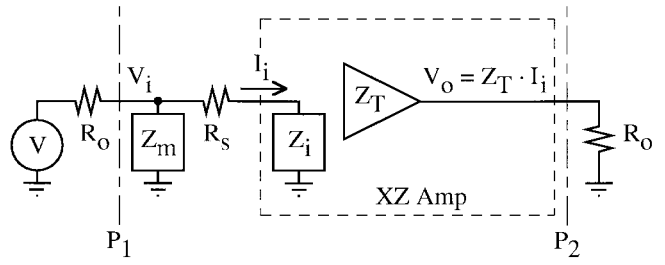


Fig. 7. Test circuit for a transimpedance amplifier with low return loss.

subsequent amplification. The XZAMP input is designed to be fed by an MSM that has high output impedance (several kiloohms) in parallel with small capacitance (about 50 fF). The high input impedance of this amplifier results in an S_{11} near one, which, as we will see, complicates characterization. The input current in the RF test must be calculated from the scattering parameters. Fig. 7 shows a conceptual model of a transimpedance amplifier of transimpedance Z_T and input impedance Z_i connected to an input network (Z_m and R_s) fed from an RF source (V in series with R_o, the system characteristic impedance). First consider the case of normal RF measurements, with Z_m infinite and zero R_s. The input current I_i can be calculated from V and S_{11}; the output voltage V_o is given by $S_{21} \cdot V/2$. Thus,

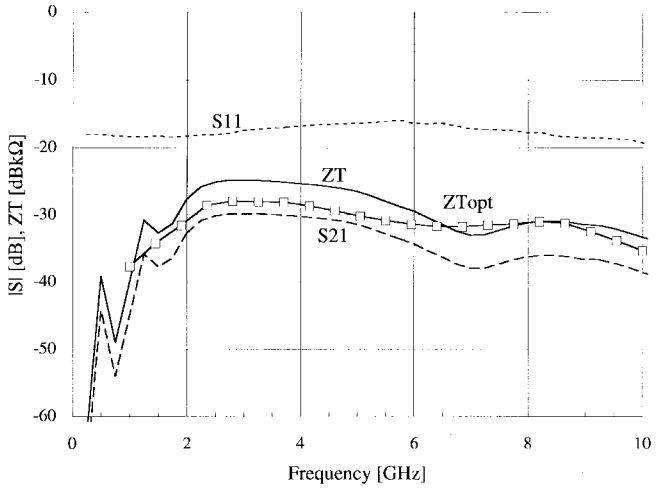
$$Z_T = R_o \cdot S_{21}/(1 - S_{11}). \tag{1}$$

With S_{11} near one, small errors in phase or amplitude of S_{11} can result in large errors in Z_T.

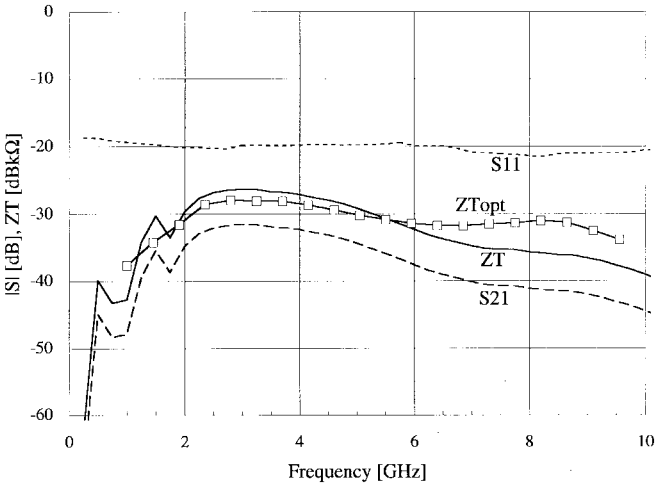
Now consider adding the matching components Z_m and R_s. Z_m is chosen to provide high return loss, while R_s is chosen large enough that $|R_s + Z_i|$ is reasonably well known. In our case, $|Z_i|$ is a few hundred Ω and we chose R_s to be 1.8 kΩ. With this network, using the reference planes shown in Fig. 7, we find that

$$Z_T = (R_s + Z_i) \cdot S_{21}/(1 + S_{11}). \tag{2}$$

We need to know $|R_s + Z_i|$ to the accuracy desired in Z_T, but now S_{11} is small and, furthermore, the result depends on it only weakly.



(a)



(b)

Fig. 8. Comparison of optical and electrical measurements made using the on-chip input matching structure. Long-dashed line: $|S_{21}|$. Short-dashed line: $|S_{11}|$. Solid line: transimpedance calculated from S parameters. Solid line with squares: transimpedance measured optically on a different chip. (a) and (b) show RF measurements on two different (nominally identical) fixtured chips.

In the following figures, the RF scattering parameters are given in decibels, phase angles in degrees, and transimpedance in dB relative to 1 kΩ, i.e., Z_T [dB $\cdot$ kΩ] is $20 \cdot \log_{10}(Z_T/1$ k$\Omega)$.

Fig. 8 shows a comparison of transimpedance measured electrically on two chips and optically on a third (the latter taken from Fig. 10). The electrical measurements are from fixtured chips configured (via their airbridges) to use the input matching structure. The values used are $Z_m = 50\ \Omega$ and $R_s = 1.8$ kΩ; $|Z_i|$ is a few hundred ohms at a phase angle near 90°. To calculate Z_T we used (2) with $|(R_s + Z_i)|$ taken as 1.8 kΩ. The agreement between Z_T and $Z_{T\mathrm{opt}}$ is good.

In Fig. 9, we show a similar comparison, using the same optical measurements but electrical measurements from yet another chip, this one using no input matching structure; (1) applies. S_{11} is near 0 dB, so the calculated Z_T depends sensitively on accurate knowledge of its phase and is seen not to agree well with $Z_{T\mathrm{opt}}$. We show by two error bars

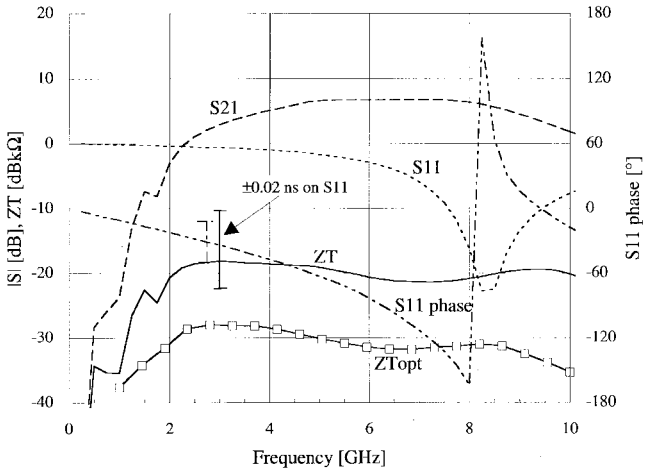


Fig. 9. Comparison of optical and electrical measurements made without using the on-chip input matching structure. Long-dashed line: $|S_{21}|$. Short-dashed line: $|S_{11}|$. Dash–dot–dot line: phase of S_{11}. Solid line: transimpedance calculated from S parameters. Solid line with squares: transimpedance measured optically on a different chip. Error bars: shift in phase of S_{11} and in calculated Z_T when a time delay (reference plane shift) of ± 0.02 ns is applied to S_{11}.

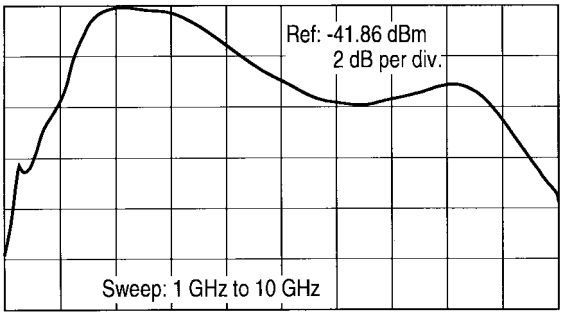


Fig. 10. RF performance with optical input.

the change in calculated phase angle of S_{11} and magnitude of Z_T when a phase shift (reference plane shift) of ± 0.02 ns is applied to the S_{11} data. This corresponds to a few mm position difference or a stray capacitance of about 0.4 pF. The large shifts in calculated Z_T result from the strong dependence of (1) on S_{11} when the input is highly mismatched (so S_{11} is near unity).

The large dip in S_{11} near 8 GHz, which was not seen in simulation while the IC was being designed, shows that there are some unmodeled parasitics in the input to the XZAMP front end. As we have just seen, such effects can be very important in characterizing a mismatched circuit. Since MSM's are quite high impedance (even the shunt capacitance of some 50 fF is in the kiloohm range at 3 GHz), a high-impedance front-end design will often be necessary. Electrical testing will then benefit greatly from an input matching structure such as we describe here.

Fig. 10 shows on-wafer measurements of the RF output with optical input. The optical source is an 830-nm DFB laser diode, fiber pigtailed to the optical input of a MZM, which modulates the intensity sinusoidally. The MZM optical output travels through a single-mode fiber and is proximity coupled to an MSM photodetector on the MOE1 wafer. The low-capacitance

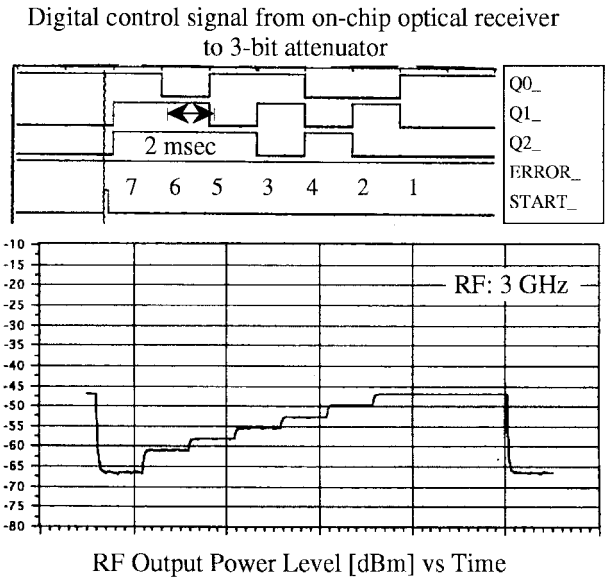


Fig. 11. Operation of the MOE1 IC. The output is from a spectrum analyzer set at a fixed frequency, 3 GHz. A 5-bit digital word is shifted into the IC over its optical fiber to change the state of the on-chip attenuator for each of the sequential output level changes shown.

(50 fF) high-responsivity (0.4 A/W) MSM has an area of 50 μm $\times$ 50 μm with 0.5-μm-wide electrodes set on a pitch of 1.5 μm. The modulation factor M (0.09 at 3 GHz) was measured independently over frequency to take into account the frequency-dependent transmission of the MZM and the RF cabling. The measured dc photocurrent was 0.7 mA. The peak RF signal level in Fig. 10 at the output of the IC is -42 dBm into 50 Ω with the optical input just described having approximately 110-μW rms of RF-modulated optical power.

To compare these measurements with the electrical ones, we note that the rms RF photocurrent is $I_{\rm dc} \cdot M/2^{1/2}$. To convert from power in dB relative to 1 mW (i.e., dBm) with system impedance R_o to transimpedance relative to 1 kΩ (i.e., dB $\cdot$ kΩ), with dc photocurrent measured in decibels $\cdot$ milliamperes (i.e., dB relative to 1 mA), we find

$$Z_T[\text{dBk}\Omega] = P[\text{dBm}] - I_{\rm dc}[\text{dBmA}] + 10 \cdot \log([2R_o/M^2] \cdot [.001\ \Omega^{-1}]) \quad (3)$$

where the last term is numerically $+10.9$ dB in a 50-Ω system. This equation was used to calculate $Z_{T\rm opt}$ in Figs. 8 and 9.

To complete the demonstration of the function of the IC, a fixtured chip was brought into the digital test lab and driven optically with a combined digital and CW 3-GHz RF signal by means of the setup used for the measurements in Fig. 10. The digital waveforms were generated using two function generators, each set up to give a single cycle of a sine wave starting respectively at 0° or 180° phase when triggered by a pulse from its corresponding one of two channels output from a word generator. Digital ones and zeros were output from the word generator and the signals from the function generators combined in a low-frequency power combiner. These LF signals were electrically combined with the RF and applied to the MZM.

Fig. 11 shows the measured output RF stepping through seven controlled states as digital words commanding them are shifted in. To accommodate the relatively slow maximum sweep rate of the spectrum analyzer used (in "zero-span" mode) to take the data shown in Fig. 11, the bit rate was slowed to a few kilobits/second, which were accepted by the on-chip asynchronous interface as expected. It takes 5 b transmitted to change from one state to the next, and only when the last bit is accepted is the control register then set to the new commanded state. As expected the RF amplitude during each state is unaffected by the digital shifting.

Measurements of link dynamic range (which depends on laser noise as well as the IC's electrical performance) were limited by the noise floor of the spectrum analyzer but were at least 40 dB. In particular, an experiment was done in which the digital data stream was repetitive so as to command no change in the RF amplitude, and no trace of any digital sidebands could be found on the RF output from the IC.

It is important to note that the gain of an externally modulated optical link is proportional to the CW optical power squared. Therefore, for a constant microwave input signal, the link gain can be increased by increasing the CW optical power. The transimpedance values (around 50 Ω) on this first-generation IC are low enough that its use in a real system would require additional amplification. This would be a straightforward RF design task since the optical signals have been converted to electrical ones with acceptable flatness of band.

IV. Conclusions

We have monolithically integrated an MSM photodetector, signal-conditioning circuitry, error-detection circuitry, digital decode circuitry and registers, and a three-block RF MMIC using a foundry-qualified GaAs MESFET process and demonstrated optically commanded digital control of an optically transmitted RF signal. We have developed a signaling protocol that is well adapted to such use and allows asynchronous serial data transmission over the same optical fiber carrying the RF. We have designed an on-chip input-matching test structure to allow accurate characterization of mismatched circuits such as typical transimpedance amplifiers, and used it to characterize the IC developed.

This project demonstrates the viability of such IC's and brings the idea of a monolithic digitally controlled photonic RF interconnect to fruition for the first time. A foundry-qualified photonic-link capability will help assure timely insertion of photonics into a wide variety of RF subsystems. The choice of 0.85-μm wavelength is the key enabling factor for this demonstration.

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Adam Kelsey, photograph and biography not available at the time of publication.

Susan E. Davis, photograph and biography not available at the time of publication.

Shiou-Lung G. Chu, photograph and biography not available at the time of publication.

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